

**WHAT IS CLAIMED IS:**

- 1           1.       A data processor for use in a wireless communication device, comprising:  
2           a processing unit;  
3           an instruction pipeline circuit;  
4           at least one processing module;  
5           a timer for generating a time-out interval; and  
6           power control logic for detecting a sleep instruction and placing the processing  
7           unit, instruction pipeline circuit and at least one processing module in a low-power state,  
8           where the power control logic is operative in response to a wake-up signal to reactivate  
9           the instruction pipeline circuit, and consequently at least one processing module only to  
10          the extent required by the wake-up signal.
  
- 1           2.       The processor of claim 1, where the instruction pipeline circuit comprises  
2           a multi-stage instruction pipeline circuit.
  
- 1           3.       The processor of claim 1, where the wake-up signal comprises a logical  
2           OR combination of one or more predetermined wake-up conditions and the time-out  
3           interval.
  
- 1           4.       The processor of claim 1, where the power control logic comprises  
2           instruction decode logic to detect the sleep instruction.
  
- 1           5.       The processor of claim 1, where the power control logic comprises branch  
2           condition logic to respond to the wake-up signal.
  
- 1           6.       The processor of claim 1, where the power control logic, having specified  
2           one or more wake-up conditions that the processing unit will respond to when in a low-  
3           power state, generates the wake-up signal upon detecting the one or more wake-up  
4           conditions or the time-out interval.
  
- 1           7.       The processor of claim 1, where the power control logic instructs the  
2           instruction pipeline circuit to complete any instructions preceding the sleep instruction.

1           8.       The processor of claim 7, where the power control logic instructs the  
2 instruction pipeline circuit to cease fetching new instructions after encountering a sleep  
3 instruction whose wake-up conditions are currently deasserted.

1           9.       The processor of claim 1, wherein the processing unit, instruction pipeline  
2 circuit and at least one processing module are formed together on a common silicon  
3 substrate using CMOS processing.

1           10.      The processor of claim 6, wherein the wake-up conditions and time-out  
2 interval are stored in a register by the power control logic.

1           11.     An article of manufacture having at least one recordable medium having  
2     stored thereon executable instructions and data which, when executed by at least one  
3     processing device, cause the at least one processing device to:  
4             detect a sleep instruction for the processing device;  
5             specify one or more wake-up conditions and a time-out interval;  
6             power down an instruction pipeline and one or more processor modules;  
7             reactivate the instruction pipeline upon detection of a wake-up signal  
8     corresponding to either a wake-up condition or the time-out interval, and  
9             process one or more instructions in the instruction pipeline to reactivate any of the  
10    one or more processor modules required to respond to a detected wake-up condition.

1           12.     The article of manufacture of claim 11, wherein the processing device  
2     executes any instructions received by the instruction pipeline before the sleep instruction  
3     is received.

1           13.     The article of manufacture of claim 11, wherein the instruction pipeline  
2     comprises a multistage instruction pipeline, and the processing device reactivates only  
3     stages in the multistage instruction pipeline and/or the function units needed to process  
4     one or more instructions necessary to analyze and respond to the wake-up signal.

1           14.     The article of manufacture of claim 11, further comprising a register for  
2     holding the specified wake-up conditions and time out signal.

1           15.     The article of manufacture of claim 11, where the processing device is  
2     implemented as part of a single-chip wireless communication device.

1           16.     The article of manufacture of claim 11, where the executable instructions  
2     and data comprise control logic for controlling the operation of the processing device.

1           17.     The article of manufacture of claim 11, where the processing device  
2     powers down the one or more processor modules by freezing a clock signal for said one  
3     or more modules.

1           18.    The article of manufacture of claim 11, where the processing device  
2 powers down the one or more processor modules by placing said one or more modules in  
3 an idle mode.

1           19.    A method for managing power in a communications processor by  
2 selectively removing one or more processor modules from a standby mode, comprising:  
3           storing one or more wake-up conditions and a time-out interval in a register;  
4           receiving a processor sleep instruction;  
5           executing any pending instructions received by the processor before the sleep  
6 instruction;  
7           powering down the one or more processor modules;  
8           receiving a processor wake-up signal corresponding to one of said wake-up  
9 conditions or said time-out interval;  
10          powering up only the processor modules required to respond to the detected  
11 processor wake-up signal.

1           20.    The method of claim 19, wherein one of the processor modules comprises  
2 an instruction pipeline circuit.